Remarks

Entry of the amendments, reconsideration of the application, and allowance of all pending claims are respectfully requested. Claims 1-14 and 30-33 are now pending.

In accordance with 37 C.F.R. §1.121(c)(1)(ii), a marked-up version of the amended claims is provided on one or more pages separate from the amendment. These pages are appended at the end of the Response.

By this amendment, non-elected claims 15-29 are canceled without prejudice. These claims may be made the subject of a separate divisional application. In addition, claim 1 is amended and new claims 30-33 are added to more particularly point out and distinctly claim the subject matter of the present invention. These amendments to the claims constitute a bona fide attempt by the applicants to advance prosecution of this application and obtain allowance of certain claims and are in no way meant to acquiesce to the substance of the initial rejection. It is believed that the amendments to the claims place all claims in condition for allowance. No new matter is added to the application by any amendment presented herewith.

Original claims 1-14 were rejected under 35 U.S.C. 112, second paragraph. In particular, the term "substantially lower" in claim 1 was objected to. In response, applicants' herein amend claim 1 to delete the word "substantially", and recite that the second solder bumps have at least a portion that melts at a lower temperature than the first solder

bumps. In view of this amendment to claim 1, applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. 112, second paragraph, rejection to the claims.

Substantively, claim 1-10 were rejected under 35 U.S.C. 102(b) as being anticipated by Dalal et al. (U.S. Patent No. 5,796,591), while claims 1 & 11-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (U.S. Patent No. 5,646,828) in view of Ikegami (U.S. Patent No. 6,137,184). These rejections are respectfully, but most strenuously, traversed to any extent deemed applicable to the claims presented herewith.

With respect to the anticipation rejection, it is well settled that a claimed invention is not anticipated unless a single prior art reference discloses: (1) all the same elements of the claimed invention; (2) found in the same situation as the claimed invention; (3) united in the same way as the claimed invention; (4) in order to perform the identical function of the claimed invention. In this instance, Dalal et al. fails to disclose at least one element of each of the independent claims and as a result does not anticipate, or even render obvious, applicants' invention.

Applicants' invention (for example, as recited in claim 1) includes a structure having a first substrate and a second substrate. First solder bumps and second solder bumps are offset between the first substrate and the second substrate. In addition to being offset, these first solder bumps and second solder bumps comprise separate solder bumps disposed between the first substrate and the second

substrate. Still further, applicants' recite that the second solder bumps have at least a portion that melts at a lower temperature then the melting temperature of the first solder bumps.

Applicants' respectfully submit that a careful reading of the Dalal et al. patent fails to uncover any teaching, suggestion or implication of at least one aspect of their above-summarized structure.

Dala et al. describe a direct chip attached circuit card wherein an IC chip 30 includes a solder bump 38 with a cap of low melting point metal 41. Solder bump 38 aligns over and connects to a copper pad 20 disposed above a laminate 10. This vertical disposition and alignment of the first solder bumps (20) and second solder bumps (38) in Dalal et al. is clearly different from applicants' invention.

Applicants recite in amended claim 1 that the first solder bumps and second solder bumps are offset between the first substrate and the second substrate. This concept is not disclosed or suggested by Dalal et al. In Dalal et al., solder bumps 38 necessarily align over and connect to copper pads 20. Thus, the solder bumps are not offset as recited by applicants (and depicted, for example, in FIG. 1 of the present application). Further, it is respectfully submitted that applicants' invention would not have been obvious in view of Dalal et al. since the vertically disposed solder bumps in Dalal et al. necessarily are aligned in order to achieve interconnection. That is, the first solder bumps and second solder bumps in Dalal et al. achieve the same

interconnection. If these solder bumps were offset as recited by applicants, then the electrical interconnection taught by Dalal et al. would not be achievable.

For the above reasons, applicants respectfully submit that there is no anticipation of claim 1 based upon the teachings of Dalal et al., nor would applicants' invention have been considered obvious by one of ordinary skill in the art based on the teachings thereof. Dependant claims 2-14 are believed allowable for the same reasons, as well as for their own additional characterizations.

For example, claim 8 recites the structure of claim 1 and adds the characterization that the second solder bumps are for aligning the first substrate and the second substrate before melting the first solder bumps. Applicants respectfully submit that a careful reading of Col. 6, lines 1-12 of Dalal et al. (cited in the Office Action) does not disclose that the second solder bumps facilitate alignment of the two substrates. The solder bumps in Dalal et al. are not being used for the purpose of alignment, but rather alignment is achieved by some other means prior to melting of the solder bumps.

Claim 10 further states that the second solder bumps melt at a temperature at least 25°C less than that of the first solder bumps. This claim is submitted as a characterization on the second solder bumps melting at a "lower temperature" than the first solder bumps. A careful review of FIG. 5 and Col. 8, lines 49-57 of Dalal et al. (cited in the Office Action), fails to uncover any suggestion or implication that the second solder bumps melt

at a temperature at least 25°C less than the first solder bumps.

New claims 30-33 are believed allowable for the same reasons as independent claim 1 and 10 noted above. Claim 30 recites a structure which includes a first substrate having a main surface with first solder bumps and second solder bumps separately disposed thereacross. The second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps in order to facilitate alignment of the first substrate to a second substrate before melting of the first solder bumps. A careful reading of Dalal et al. (as well as the other applied art) fails to uncover any teaching, suggestion or implication of such a structure or function.

As noted, claims 1 & 11-14 were rejected as obvious over Degani et al. in view if Ikegami. Reversal of this rejection is also requested in view of the amendments submitted herein.

An "obviousness" determination requires an evaluation of whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art. In evaluating claimed subject matter as a whole, the federal circuit has expressly mandated that functional claim language be considered in evaluating the claim relative to the prior art. Applicants respectfully submit that the application of these standards to the independent claims submitted herewith leads to the conclusion that the recited subject matter would not have

been obvious to one of ordinary skill in the art based on the applied patents.

Degani et al. discloses a multi-chip module having enhanced thermal/power management. First and second substrates 18 & 19 appear to be interconnected by solder bumps. The solder bumps are not labeled in the patent or even discussed in the specification. The Office Action alleges that one solder bump contacts the land or pad 21 thereby defining first solder bumps. Reconsideration of this position is requested.

First, applicants clearly recite first solder bumps and second solder bumps. That is, applicants recite two sets of bumps. In Degani et al., the figures only show one bump contacting land 21 between chip 19 and chip 18. Thus, the drawings do not teach, using the Examiner's characterization, first solder bumps and second solder bumps. In addition, applicants respectfully submit that there is no teaching, suggestion or implication in Degani et al. to characterize the solder bumps depicted therein as being different structures. By comparison, in applicants' invention the first and second solder bumps are necessarily different structurally in order that the second solder bumps melt at a lower temperature than the first solder bumps. In applicants' invention, the grouping of solder bumps into the first and second sets is structurally related.

The Office Action's characterization of first solder bumps and second solder bumps in Degani et al. is an artificial characterization made in hindsight and not based on the structure of the bumps themselves. In Degani et al.,

there is no teaching or suggestion that the solder bumps have different compositions. Since there is no discussion in Degani et al. that the bumps comprise inherently different structures, then applicants respectfully request reconsideration and withdrawal of the obviousness rejection to these claims based upon Degani et al. and Ikagami.

The Office Action recognizes that Degani et al. does not disclose second solder bumps which have at least a portion that melts at a lower temperature then the first solder bumps. For a teaching of this deficiency, the patent to Ikagami is referenced.

Ikagami discloses a flip-chip type semiconductor device which has recessed-protruded electrodes in a press-fit contact. A bump electrode 4 (comprising solder) and a pad electrode 10 are aligned and interconnected as shown, for example, in FIG. 3.

Applicants respectfully submit that a careful reading of Ikagami fails to disclose many features of applicants' invention when applied against the independent claims presented herewith. For example, the bumps and electrodes in Ikagami are aligned, and therefore, would not be offset as recited by applicants in claim 1. Further, there is no teaching, suggestion or implication in Ikagami of second solder bumps, having at least a portion that melt at a lower temperature, which facilitate aligning of a first substrate and a second substrate as recited by applicants in claim 30.

In addition, applicants respectfully traverse the combination of Degani et al. and Ikagami. Applicants submit

that a prima facie case of obviousness is not stated by the combination of Degani et al. and Ikagami given the different dispositions and functions of the alleged first solder bumps and second solder bumps in the two patents. As noted above, the Office Action characterizes the horizontally disposed solder bumps in Degani et al. as first solder bumps and second solder bumps, since one solder bump connects to a pad 21 disposed between chip 19 and chip 18. In contrast, the teachings of Ikagami refer to a solder bump and a pad vertically disposed and aligned to establish electrical connection between two devices. A careful reading of Degani et al. and Ikagami fails to uncover any suggestion why one or ordinary skill in the art would assume that the first and second solder bumps in Ikagami could be offset or separated horizontally (as allegedly referenced in Degani et al.), and yet somehow facilitate electrical connection as asserted in the Office Action.

For all of the above reasons, applicants respectfully submit that the independent claims presented herewith patentably distinguish over Degani et al. in view of Ikagami. Reconsideration and withdrawal of the obviousness rejection is therefore respectfully requested. The independent claims are believed allowable for the same reasons as independent claims, as well as for their own additional characterizations.

For the above reasons, applicants respectfully request reconsideration and allowance of all claims presented herewith.

Applicants' undersigned attorney is available, should the Examiner wish to discuss this application further.

Respectfully submitted,

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Version with markings to show changes made

In the Claims:

Claim 1 has been amended, as follows:

1. (AMENDED) A structure comprising:

a first substrate and a second substrate; and

first solder bumps and second solder bumps offset therebetween, wherein said first solder bumps and said second solder bumps comprise separate solder bumps disposed between said first substrate and said second substrate, and wherein said second solder bumps have at least a portion that melts at a [substantially] lower temperature than said first solder bumps.

Claims 15-29 have been canceled.

New claims 30-33 have been added, as follows:

30. (NEW) A structure comprising:

a first substrate having a main surface with first solder bumps and second solder bumps separately disposed thereacross; and

wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps, said second solder

bumps being for aligning said first substrate to a second substrate before melting said first solder bumps.

31. (NEW) The structure of claim 30, wherein said second solder bumps are larger than said first solder bumps.

32. (NEW) The structure of claim 30, wherein said second solder bumps melt at a temperature at least 25°C less than said first solder bumps.

33. (NEW) The structure of claim 32, wherein the first substrate comprises a semiconductor chip.